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(54) **MEMORY USABLE IN CACHE MODE OR SCRATCH PAD MODE TO REDUCE THE FREQUENCY OF MEMORY ACCESSES**

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(57) **ABSTRACT**

A processor adapted to couple to external memory. The processor comprises a controller and data storage (e.g., cache memory). The data storage is configurable to operate in either a cache policy mode in which a miss results in an access of the external memory or in a scratch pad policy mode in which a miss does not result in an access of the external memory. The data storage comprises a first portion and a second portion, and only one of the portions is active at a time. The non-active portion is unusable to store or retrieve data (e.g., Java local variables). When the active portion does not have sufficient capacity for additional data to be stored therein, the other portion becomes the active portion.

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